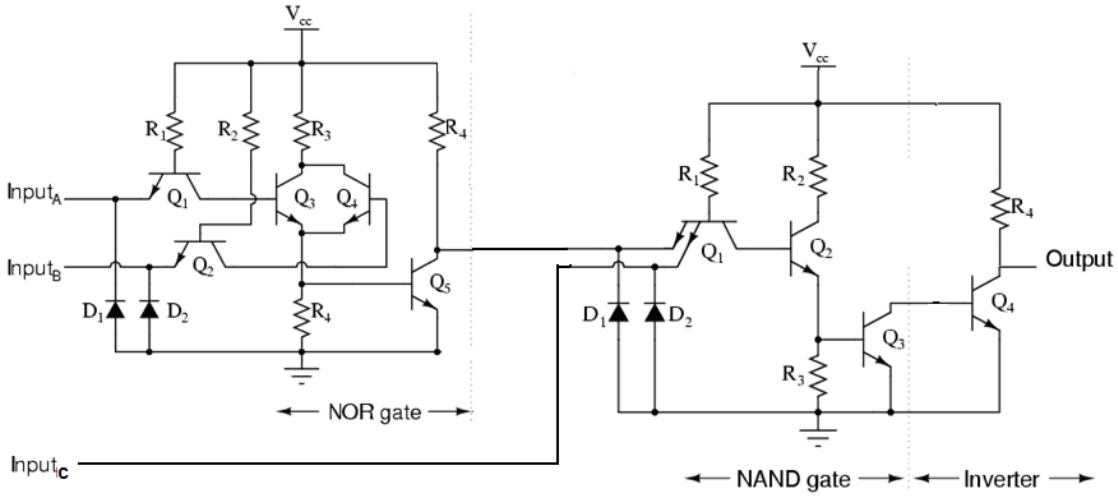
/ECE 329 FINAL EXAM
QUESTIONS

1(22p)	2a(11p)	2b(11p)	2c(0p)	2d(11p)	3(16p)	4(16p)	5(16p)	6(16p)	7(16pts)

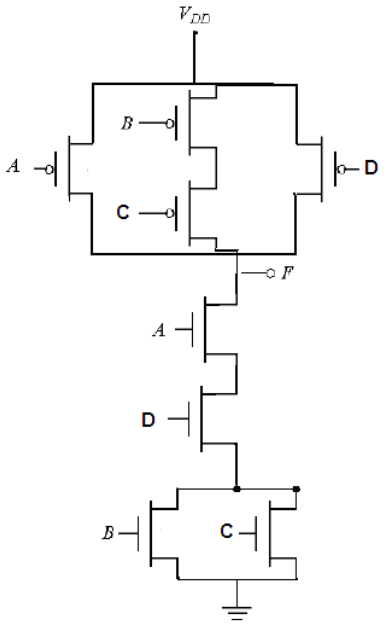
1) **(22 p)** Design a circuit with TTL (Transistor – Transistor Logic) that implements F= (A+B)'.C

Solution



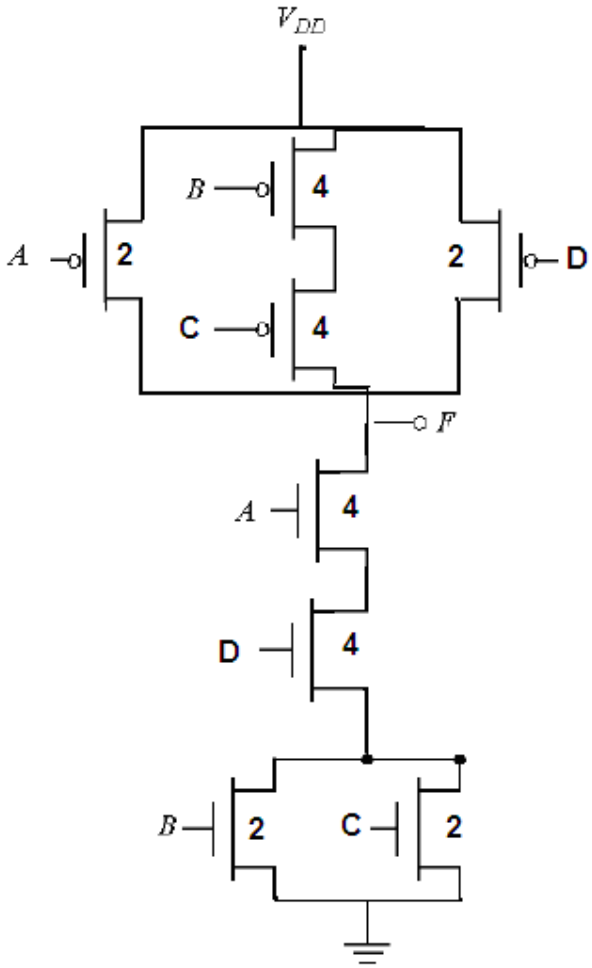
2) a) **(11 pts)** Design a circuit with CMOS (Complementary Metal Oxide Semiconductor) that implements F= (A.((B+C).D))'

Solution



b) **(11 pts)** Design the sizing of the NMOS / PMOS transistor of F= (A.((B+C).D))' as ½

Solution



c) **(0 pts)** Calculate the Logical Efford of F= (A.((B+C).D))'

Solution

g = 1 for an inverter pmos/nmos =2/1 (2+1=3 C unit)

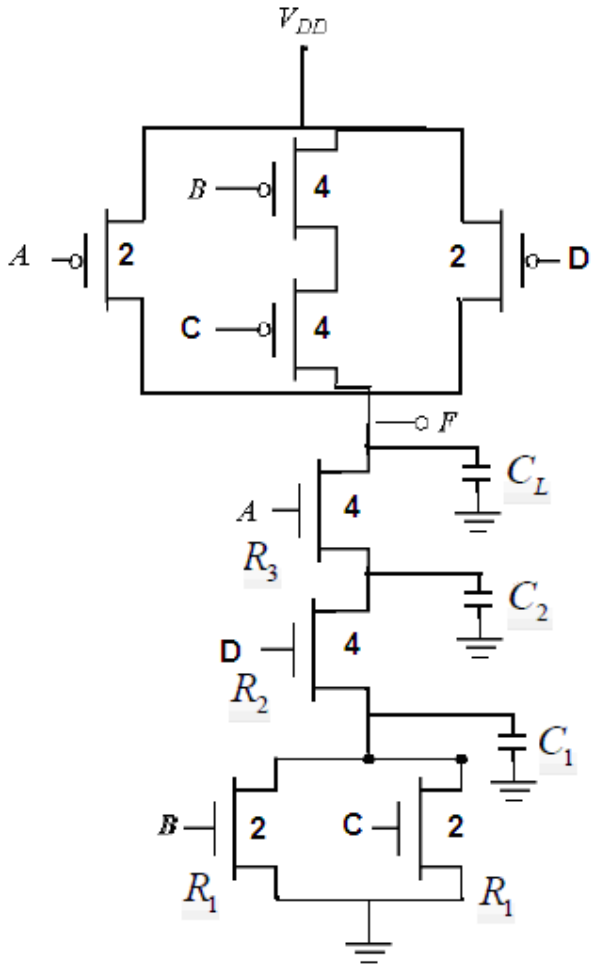
g_f = (4 C unit + 4 Cunit)/ 3 C unit = 8/3

CANCELLED (the answer was forgetten to be erased before the exam)

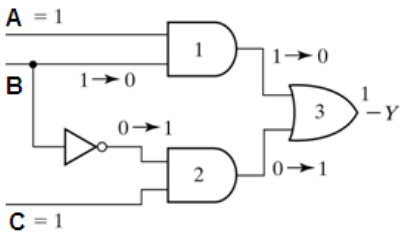
d) **(11 pts)** Calculate the Elmore Delay assuming all the transistors have equal size.

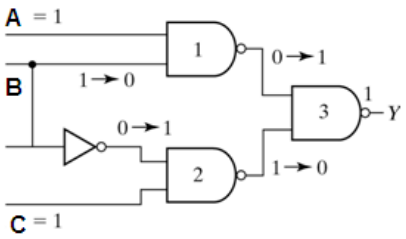
Solution

$$t_{pHL} = 0.69\left[R_1C_1 + (R_1 + R_2)C_2 + (R_1 + R_2 + R_3)C_L\right]$$

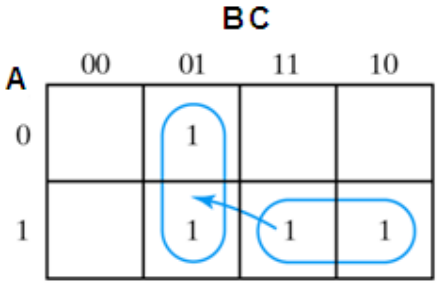


3) **(16 pts)** For the function F= AB+ B'C, the hazards are illustrated below, design a hazard free circuit that generates results for same function.

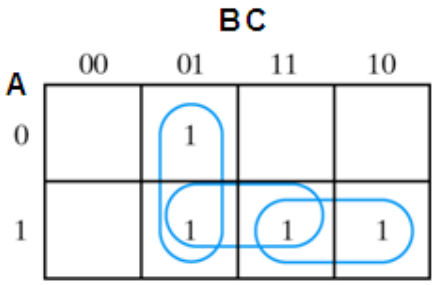




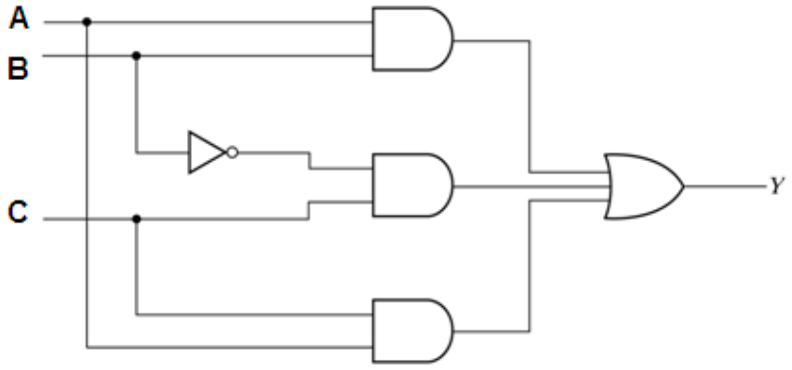
Solution



(a) Y=AB+B'C



(b) Y=AB+B'C+AC



Hazard-Free Circuit

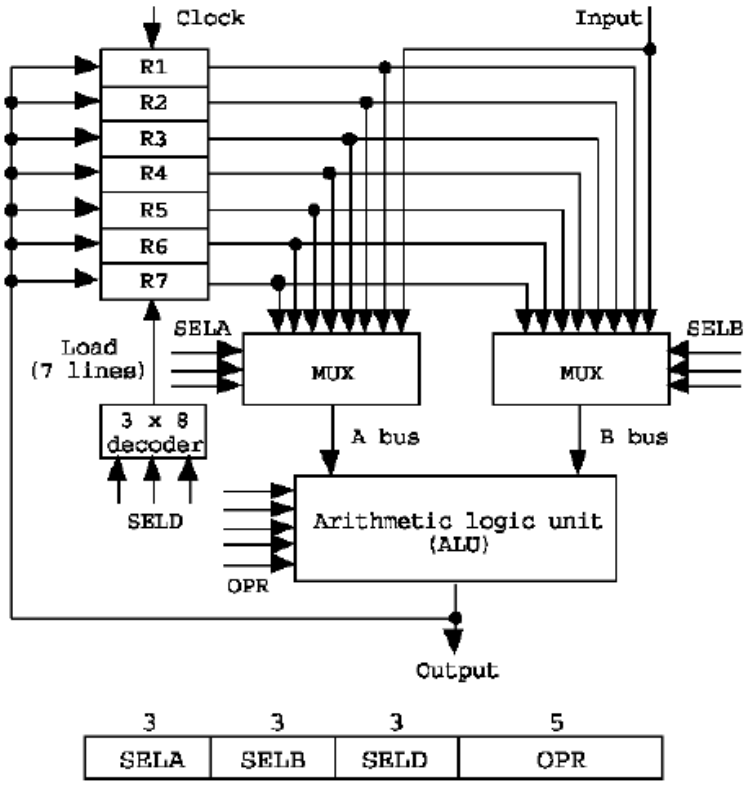
4) **(16 pts)** Encoding of the Register selection fields, Encoding of the ALU and structure of CPU communication are given below,

- Encoding of the register selection fields

Binary code	SELA	SELB	SELD
000	External input	External input	External input
001	R1	R1	R1
010	R2	R2	R2
011	R3	R3	R3
100	R4	R4	R4
101	R5	R5	R5
110	R6	R6	R6
111	R7	R7	R7

- Encoding of the ALU operation field

OPR select	Operation	Symbol
00000	Transfer A	TSFA
00001	Increment A	INCA
00010	Add A + B	ADD
00101	Subtract A - B	SUB
00110	Decrement A	DECA
01000	AND A and B	AND
01010	OR A and B	OR
01100	XOR A and B	XOR
01110	Complement A	COMA
10000	Shift right A	SHRA
11000	Shift left A	SHLA



According to all these given figures, explain the operations by giving the opr code values when the operations below are operated in CPU

R1 <- R1 + 1
R2 <- R1 - R3

Solution

R1 <- R1 + 1

SEL A= 001 (The value of R1 will be read)
OPR = 00001 (The value will be increased)
SEL D = 001 (The resulting value will be stored to R1 again)

R2 <- R1 - R3

SEL A= 001 (The value of R1 will be read)
SEL B= 011 (The value of R1 will be read)
OPR = 00101 (R1-R3 will be operated)
SEL D = 010 (The resulting value will be stored to R2)

5) **(16 pts)** For the pipelining belove if there exists any pipeline conflict, determine where it is and draw the new table such that the conflict is destroyed

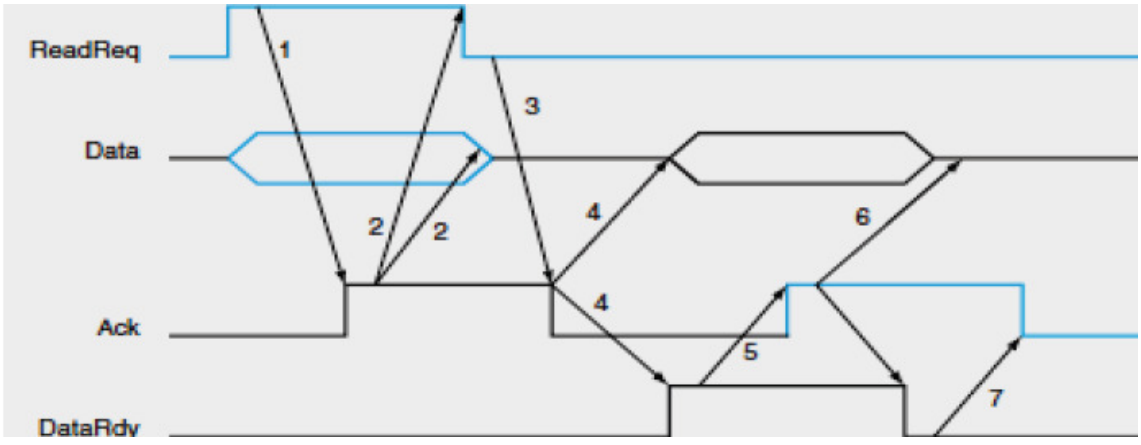
Clock cycles :	1	2	3	4	5	6
1. Load R1	I	A	E			
2. Load R2		I	A	E		
3. Add R1+R2			I	A	E	
4. Store R3				I	A	E

Solution

Clock cycles :	1	2	3	4	5	6
1. Load R1	I	A	E			
2. Load R2		I	A	E		
3. Add R1+R2			I	A	E	
4. Store R3				I	A	E

Clock cycles :	1	2	3	4	5	6	7
1. Load R1	I	A	E				
2. Load R2		I	A	E			
3. No-operation			I	A	E		
4. Add R1+R2				I	A	E	
5. Store R3					I	A	E

6) **(16 pts)** Write down the expla,nat,opn of the steps after the device signals a request by raising ReadReq and putting the address on the data lines

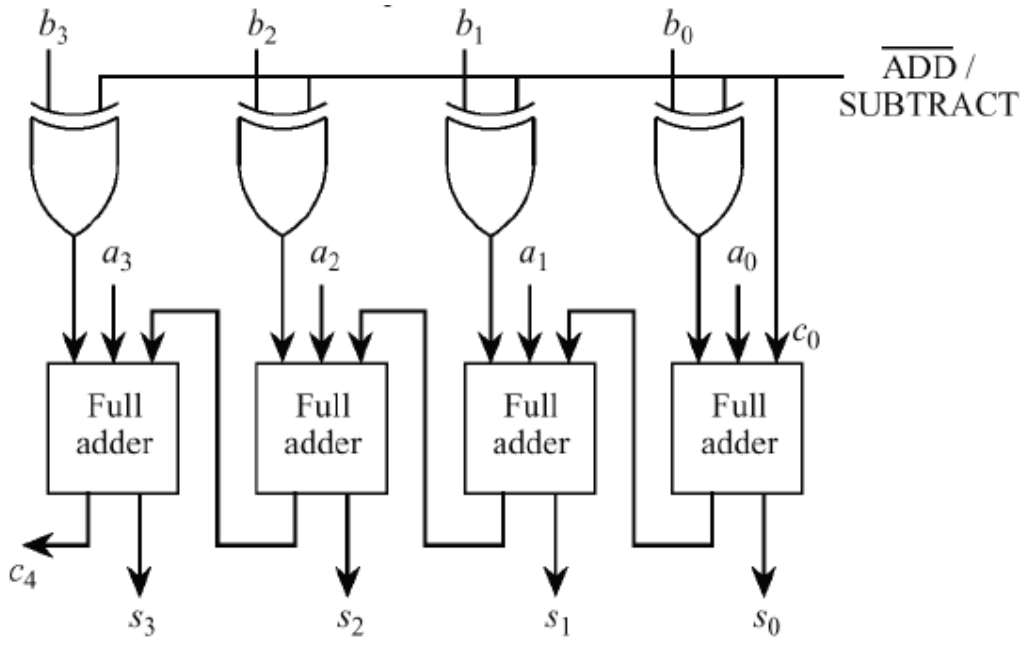


1. When memory sees the ReadReq line, it reads the address from the data bus and raises Ack to indicate it has been seen.
2. As the Ack line is high - I/O releases the ReadReq and data lines.
3. Memory sees that ReadReq is low and drops the Ack line to acknowledge the ReadReq signal (Mem. Reading in progress now).

4. This step starts when the memory has the data ready. It places the data from the read request on the data lines and raises DataRdy.
5. The I/O device sees DataRdy, reads the data from the bus, and signals that it has the data by raising Ack.
6. On the Ack signal, M/M drops DataRdy, and releases the data lines.
7. Finally, the I/O device, seeing DataRdy go low, drops the Ack line, which indicates that the transmission is completed.

7) **(16 pts)** Design and draw a combined adder subtructor

Solution



Name Surname :
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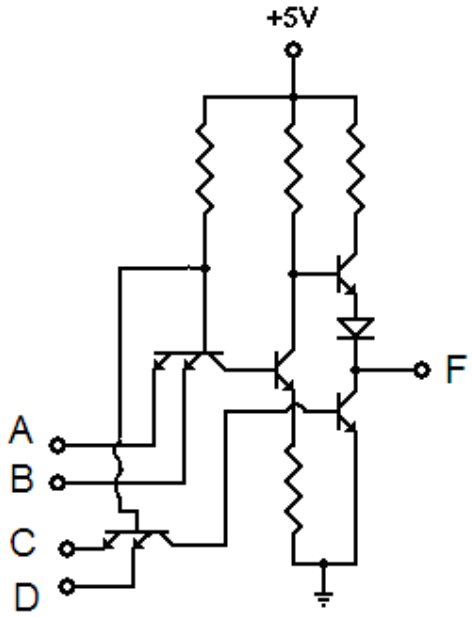
16.01.2014

ECE 329
FINAL EXAM QUESTIONS

1) **35 p** Design a CMOS circuit such that;

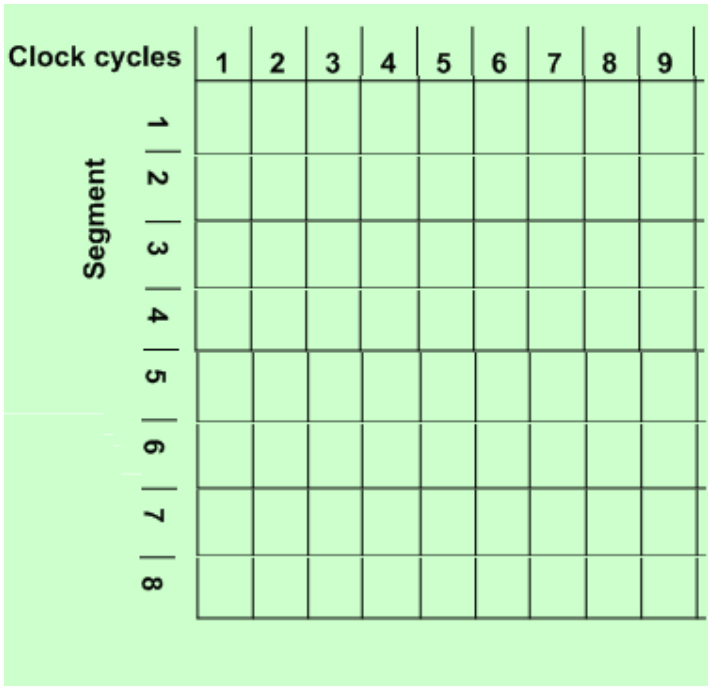
   a) **5 p** The circuit will implement F= (7,11,15) in it's simplest form
   b) **15 p** The PMOS/NMOS inverter sizing ratio will be used as 2
   c) **15 p** Assuming each PMOS resistance is inversely proportional to it's size and assuming each PMOS with size 1 has a resistance of 4 unit ohms, the equivalent resistance of PMOS side will be 1/3 unit ohms

2) **25 p** Determine the function of the given TTL cct and design the CMOS circuit which implements the same function with the following TTL circuit

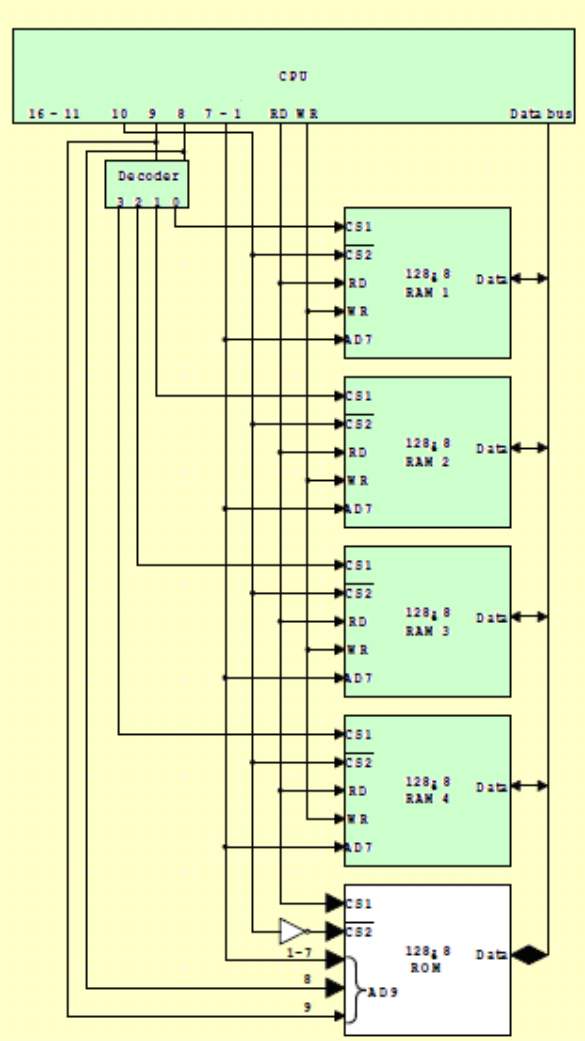


3) **25 p** Assuming variable a uses R1, variable b uses R2, variable c uses R3 and variable d uses R4 fill in the pipelining table such that there will be no conflict.

```
a=3
b=scanf("%d,&x)
c=a+b;
d=c+a;
```



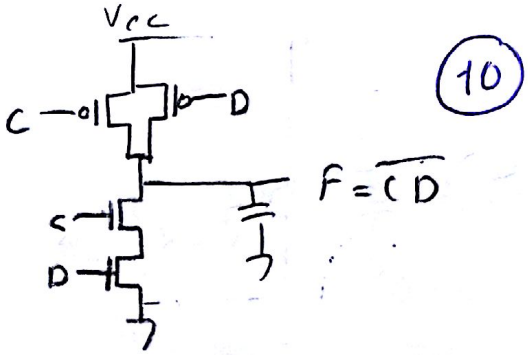
4) **15p**



Make a detailed explaination about what happens when the 16 bits +2 bitscode at the top of the figure is given to the system as seen below.

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	RD	WR
0	1	1	1	0	0	0	0	1	1	0	1	0	1	1	1	0	1

so $F = \overline{CD}$ (10) and can be drown by CMOS's as shown below



(10)

3)

clock cycles

	1	2	3	4	5	6	7	8	9
1	I	A	E						
2		I	A	E					
3			-	-	-			25	
4				I	A	E			
5					-	-	-		
6						I	A	E	
7									
8									
9									

I: Instruction Fetch

A: Address Decoding

E: Execute

4) WR = 1 } Makes write operation to
RO = 0 }

(5)

7-1 = 1 0 1 0 1 1 1 = $2^6+2^4+2^2+2^1+2^0$ = 87. Line of
or (1 1 1 0 1 0 1 = $2^6+2^5+2^4+2^2+2^0$ = 117.)

9-8 = 01 ⟶ Ram 01 (2nd RAM) → (or to 3rd RAM)
(selected by decoder) (5)

10 = 0 ⟶ ROM is out of service
RAM's are in operation (5)

so; this commends, writes data to 87.th line of RAM 01 (or 117th line of

SOLUTIONS

Name Surname :

Date :18.05.2016

ID:

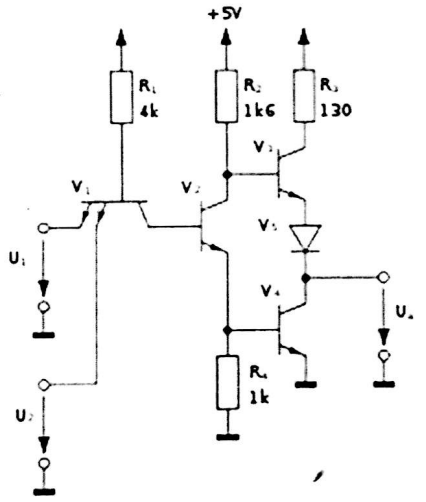
EE 214 FINAL EXAM

1)

A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

A) Design a CMOS circuit for the truth table above
B) adjust the sizing according to a Pmos/Nmos =5/3 inverter
C) and then calculate the Tp_{HL} and Tp_{LH} seperately,

2) Considering U1, U2 are inputs and Ua is output, Draw the Cmos Equivalent of the given TTL circuit below

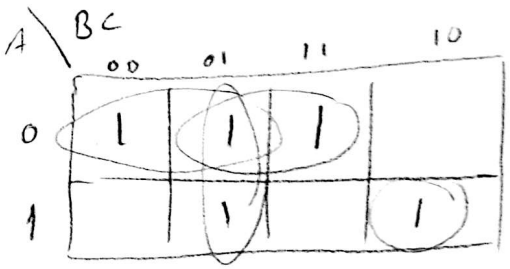


3) Draw the ASM chart of the system for which a dice is thrown and all the results are always added the results will be set to even or add after each throwing. i.e, if 2,3,4, and 1 are thrown respectively; the states will be updated as;

2 -> 2 even (0)
3 -> 5 odd (1)
4 -> 9 odd (1)
1 -> 10 even (0)

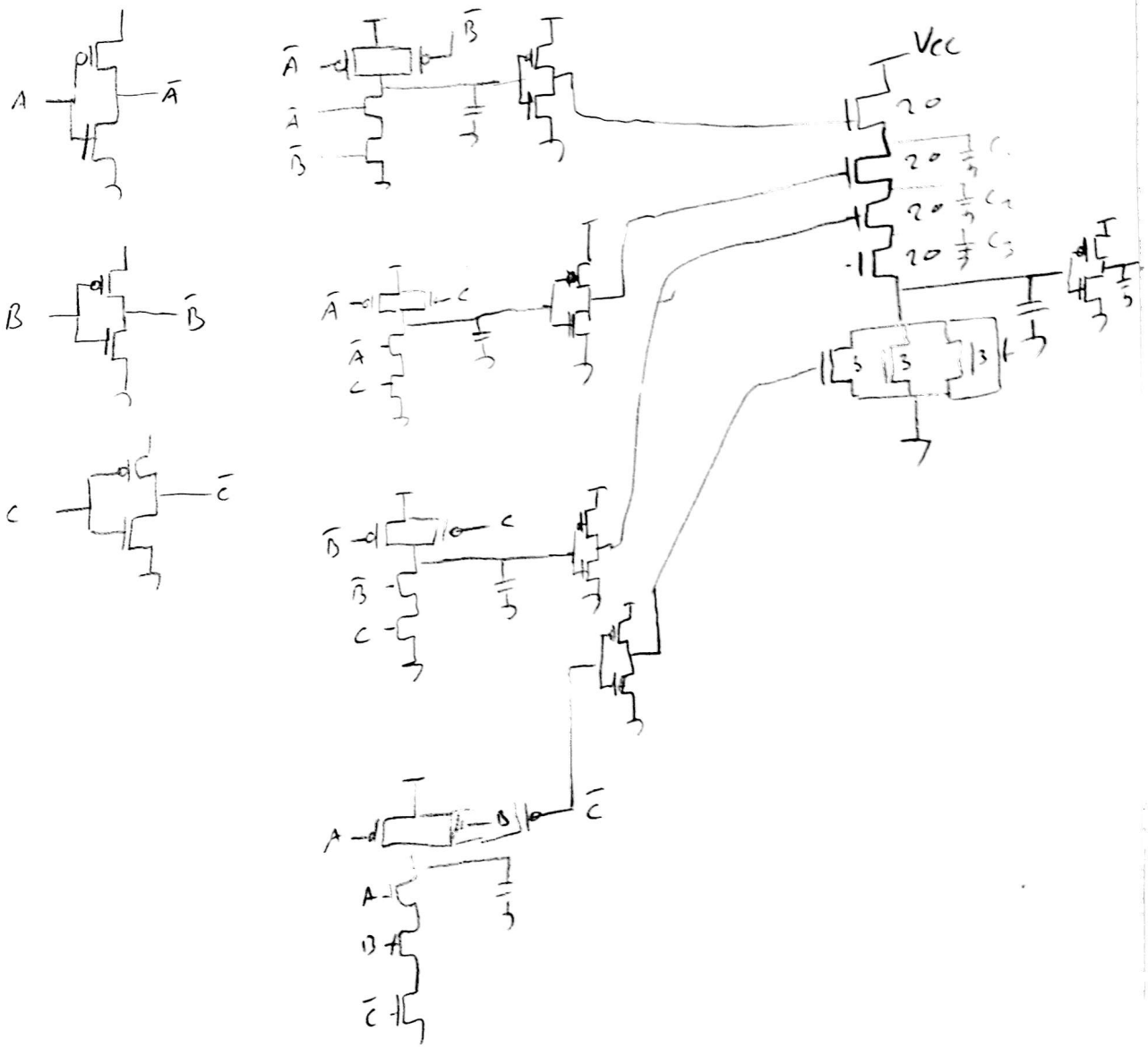
4) Design a counter that starts from 0 and counts numbers up to 31, then counts the odd numbers down from 31 to 1.

1)



$$F = \bar{A}\bar{B} + \bar{A}C + \bar{B}C + AB\bar{C}$$

a), b)



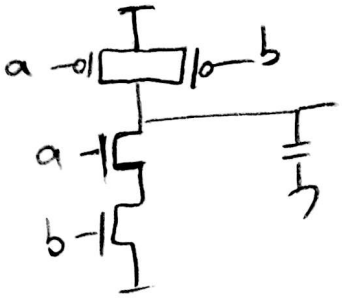
c) $t_{PHL} = 0{,}69 (R_n/3 \cdot C_L)$

$t_{PLH} = 0{,}69 (3 R_p \cdot C_1 + 2 R_p C_2 + R_p C_3 + \dots + 2_p \cdot C_L)$

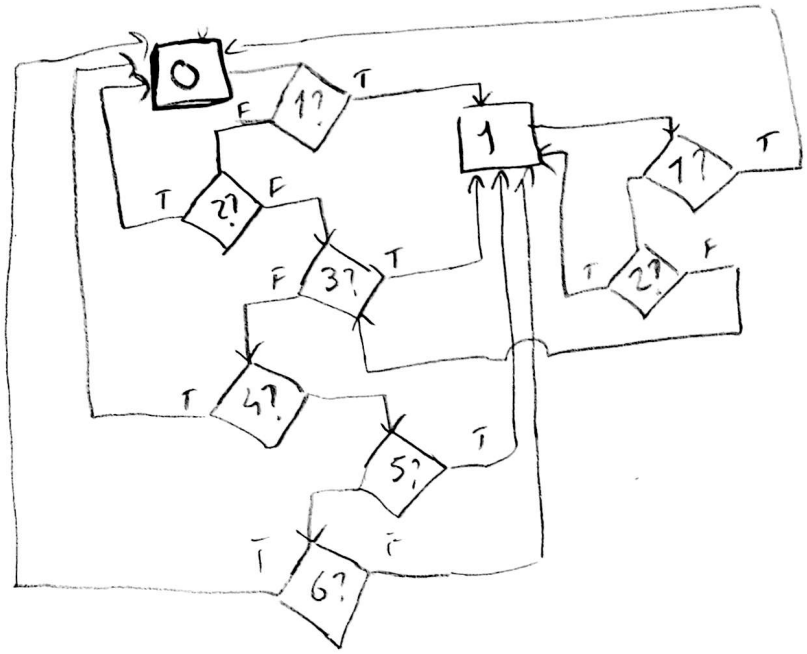
2) Truth table

a	b	F
0	0	1
0	1	1
1	0	1
1	1	0

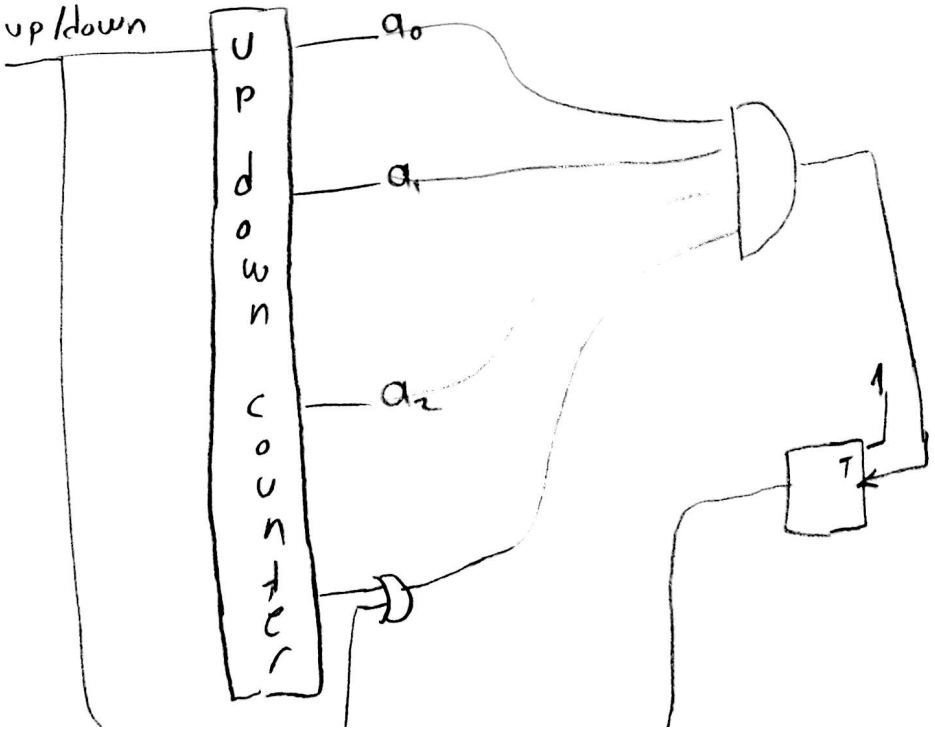
NAND



3)



4)



Name Surname:
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22.05.2017

EE 214 DIGITAL DESIGN II

FINAL EXAM.

1) Design a traffic Lamp that indicates red light for 10 seconds then indicates red and yellow lights simultaneously for 3 seconds then shows green light for 15 seconds which blinks at last 5 secs of 15 seconds.

2) Assume a system which retrieves unlimited number of numbers from the user and indicates whether the maximum of them is even or odd. Please drow the state diagram and ASM chart for this system.

3) Evaluate the results of given calculations in binary for where all in signed form numbers.

   a) $10 - 13 = -3$
   b) $13 - 10 = 3$
   c) $-10 - 13 = -23$
   d) $10 + 13 = 23$

4) a) Design a CMOS circuit for $F = \Sigma(1, 2, 6, 8, 13)$
   b) Assign their sizes such that PMOS / NMOS sizing ratio will be set to 5/3
   c) Calculate the t_{PLH} and t_{PHL} values for this circuit in terms of R_P's, R_N's, C_L's and C_{int}'s.

Name Surname:
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22.05.2017

EE 214 DIGITAL DESIGN II

FINAL EXAM.

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SOLUTIONS

25.05.2018

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EE 214 Digital Design II

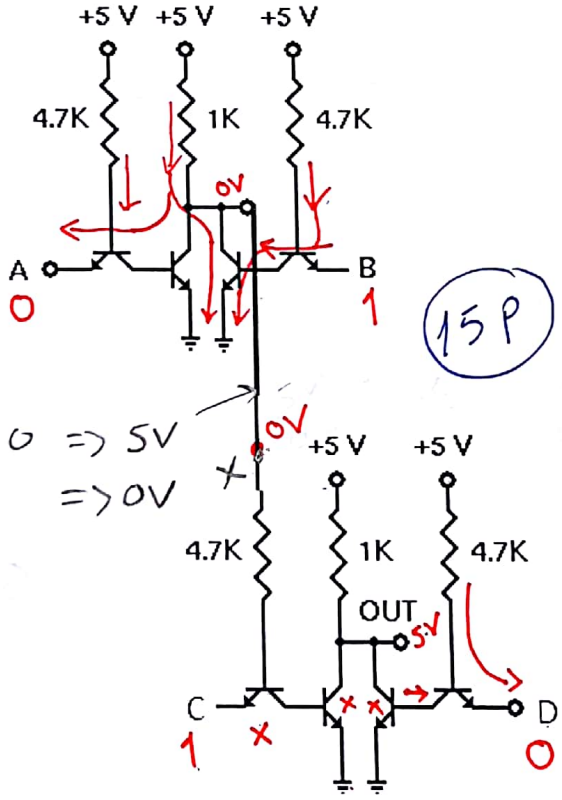
Final Exam

Q1) a) 15p Design a CMOS circuit that implements F=(A+B)C+AB(C+D)+D without simplification

b) 10p Adjust the sizes of the CMOS such that PMOS/NMOS =3/2

c) 20p Assuming that each NMOS with size 36 has 1 ohm resistance write the delay formula for the desined circuit that calculates the Tp_{LH} and Tp_{HL}

Q2) 25p Draw the truth table of the circuit for the inputs A,B,C,D. And draw the current directions for all branches of the circuit for A=0, B=1 C=1 D=0



A	B	C	D	F	
0	0	0	0	1	
0	0	0	1	0	
0	0	1	0	0	5P
0	0	1	1	0	
0	1	0	0	1	
0	1	0	1	0	
0	1	1	0	1	
0	1	1	1	0	5P
1	0	0	0	1	
1	0	0	1	0	
1	1	1	0	1	
1	1	1	1	0	

(X = 5V, C = 0V, D = 0V) => 5V

X = 0V, D = 0V => 5V

X = 0V, D = 5V => 0

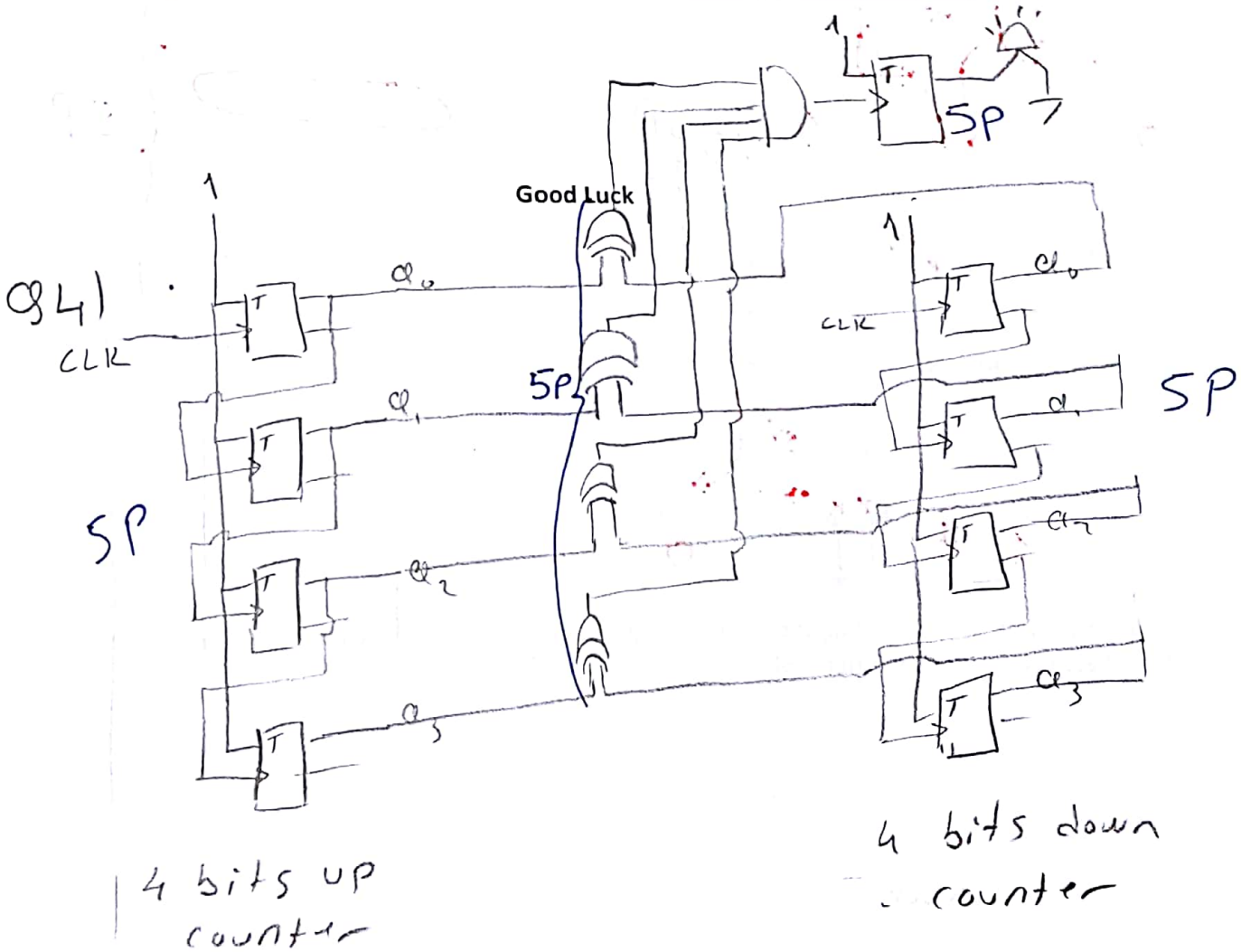
Q3) 15p For the instruction pipeling shown on the figure below, how can the runtime b increased by 20% . Please show it on an other table

3,4 will be overwritten on 6 7

Clock cycles :	1	2	3	4	5	6	7	8	9	10
1. Load	I	A	E							
2. Increment		I	A	E						
3. Add			I	A	E					
4. Subtract				I	A	E				
5. Branch to X					I	A	E			
6. No-operation						I	A	E		
7. No-operation							I	A	E	
8. Instruction in X								I	A	E

15 P

Q4) 20p Design a circuit that gives an alarm by turning on a led light when a 4 bits up counters all bits are exactly different than corresponding bits of other 4 bits down counter until next match and then turns it of after that match until the other match... continues like this...



Name Surname : **29.05.2019**

ID :

EE 468 COMPUTER ARCHITECTURE FINAL EXAM

1) **(25 p)** Please write the meanings of the words given below

Velotile Memory :

Associated Memory :

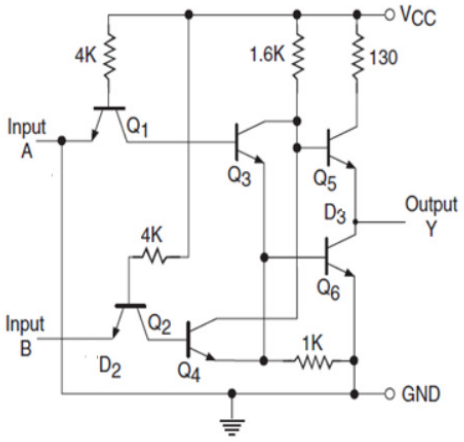
Virtual Memory :

2) **(5 p)** a) Design a CMOS circuit that implements F= a.b'+ abc +a'b

(10 p) b) Adjust the sizes of the circuit in a) for 4/3 inverter nmos/pmos sizing ratio

(15 p) c) Calculate the logical efford (g) for the circuit

3) **(20 p)** Evaluate the truth table for the given TTL circuit below



4) **(25 p)** Please make necessary operations or reorderings to overcome the conflictions of pipelining below. Show your results in the second table.

Order	1	2	3	4	5	6	7	8	9	10	11
R1=3	I	A	E								
R2=5		I	A	E							
R3=R1+R2			I	A	E						
R2=R3					I	A	E				
R5=R2+7						I	A	E			

Order	1	2	3	4	5	6	7	8	9	10	11
	I	A	E								
		I	A	E							
			I	A	E						
					I	A	E				
						I	A	E			
							I	A	E		
								I	A	E	
									I	A	E

Name Surname :

ID :

29.05.2019

EE 468 COMPUTER ARCHITECTURE FINAL EXAM

1) **(25 p)** Please write the meanings of the words given below

Velotile Memory : Temporary memory that loses content when off

Associated Memory : The memory of CPU

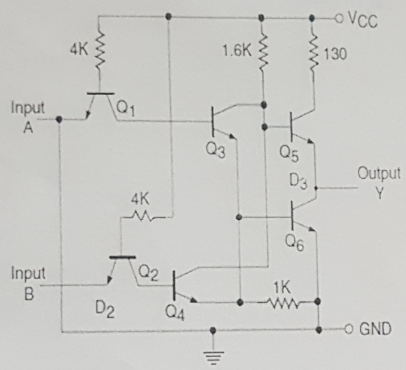
Virtual Memory : Part of HDD used as RAM

2) **(5 p)** a) Design a CMOS circuit that implements F= a.b'+ abc +a'b

(10 p) b) Adjust the sizes of the circuit in a) for 4/3 inverter nmos/pmos sizing ratio

(15 p) c) Calculate the logical efford (g) for the circuit

3) **(20 p)** Evaluate the truth table for the given TTL circuit below



A	B	F
0	0	1
0	1	1
1	0	0
1	1	0

20

4) **(25 p)** Please make necessary operations or reorderings to overcome the conflictions of pipelining below. Show your results in the second table.

Order	1	2	3	4	5	6	7	8	9	10	11
R1=3	I	A	E								
R2=5		I	A	E							
R3=R1+R2			I	A	E						
R2=R3					I	A	E				
R5=R2+7						I	A	E			

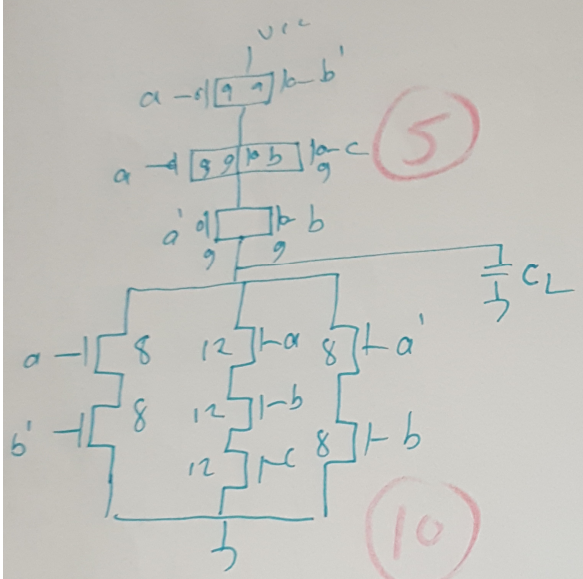
Order	1	2	3	4	5	6	7	8	9	10	11
R1=3	I	A	E								
R2=5		I	A	E							
No-op			I	A	E						
R3=R1+R2					I	A	E				
No-op						I	A	E			
R2=R3							I	A	E		
No-op								I	A	E	
R5=R2+7									I	A	E

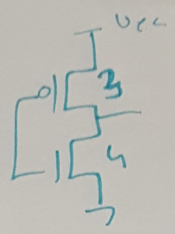
5

10

10

2)





7 unit $g=1$

21 unit x

$$x = \frac{21}{7} = 3$$

$g=3$

15

EE 468 FINAL EXAM QUESTIONS 16th JUNE 2021

Q1)

a) Please design CMOS (Complementary Metal Oxide Semiconductor) circuit that **EXACTLY** implements F= ((a.b.c)+d)'

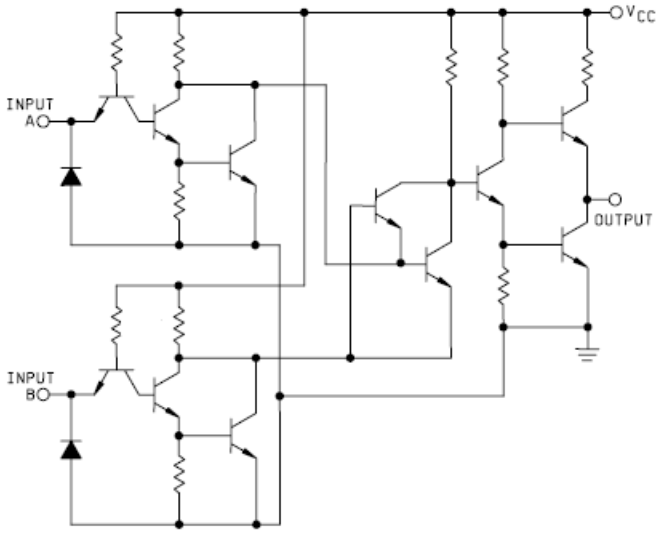
b) Please adjust the sizing of the same circuit such that rate of PMOS/NMOS =3/2.

c) Please resize all the transistors of the same circuit such that rate of PMOS/NMOS is still 3/2. But equivalent impedance (resistance) of PDN is doubled.

Q2) Fill the table given below such that if there exists any hazard for any of the functions and which minterm(s) should be added to the function to remove the hazard if there is. If there exists no hazard please write no hazards, empty rows will get no credit.

The Function	Hazard Exists (tick or cross)	Extra minterm 1 (if needed)	Extra minterm 2 (if needed)
F= a'c'+ac			
F=a'c'+a'b			
F=a'c'+abd			
F= a'c'+abc			

Q3) Please fill the truth table for the given TTL circuit. And show the arrow directions on the diagrams for A=1, B=0 case



A	B	OUTPUT
0	0	
0	1	
1	0	
1	1	

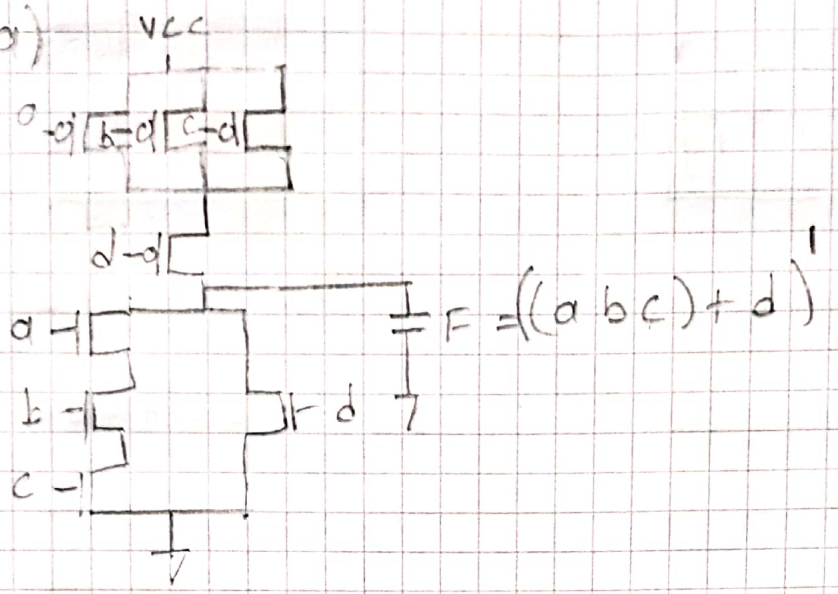
☺ GOOD LUCK ☺

EE 468

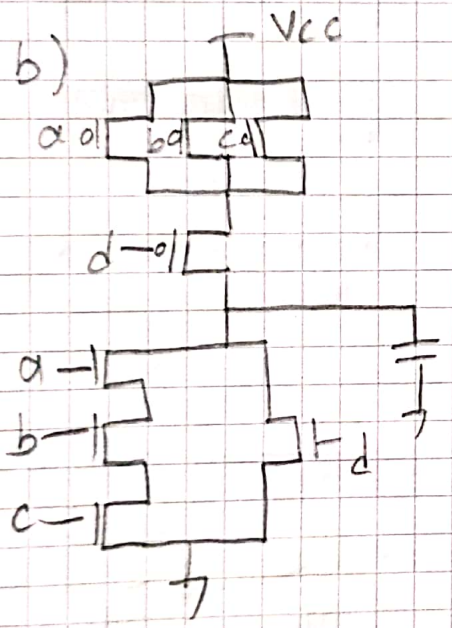
2020-2021

FINAL SOLUTIONS

1) a)



b)



PMOS / NMOS = 3/2

a = b = c = 6

d = 6

a = b = c = 6

d = 2

c) To double the resistance sizes must be divided by 2 so all the sizes must be half of its original value

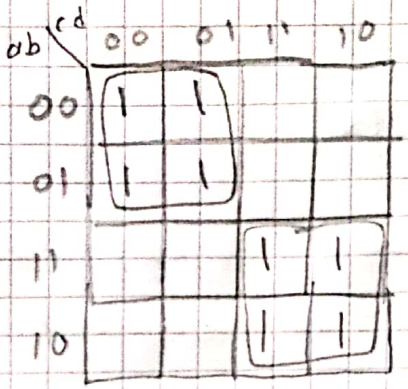
in PMOS a = b = c = 3

d = 3

in NMOS a = b = c = 3

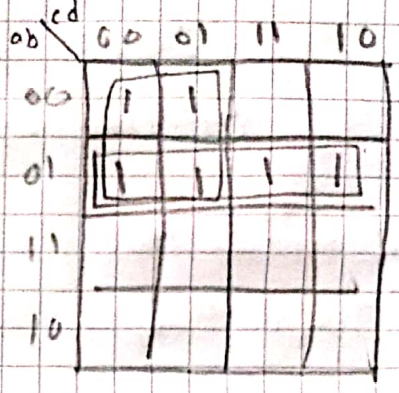
d = 1

2) a) $F = a'c' + ac$



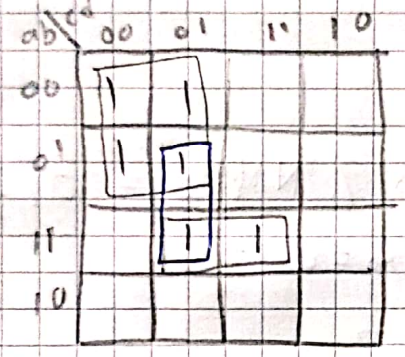
No Hazard

b) $F = a'c' + a'b$



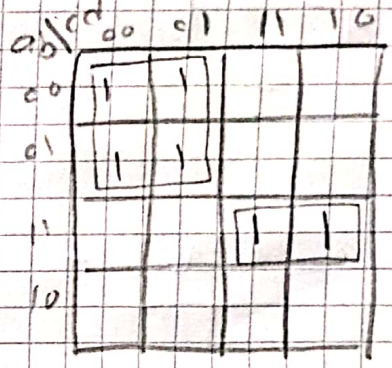
No Hazard

c) $F = a'c' + abd$



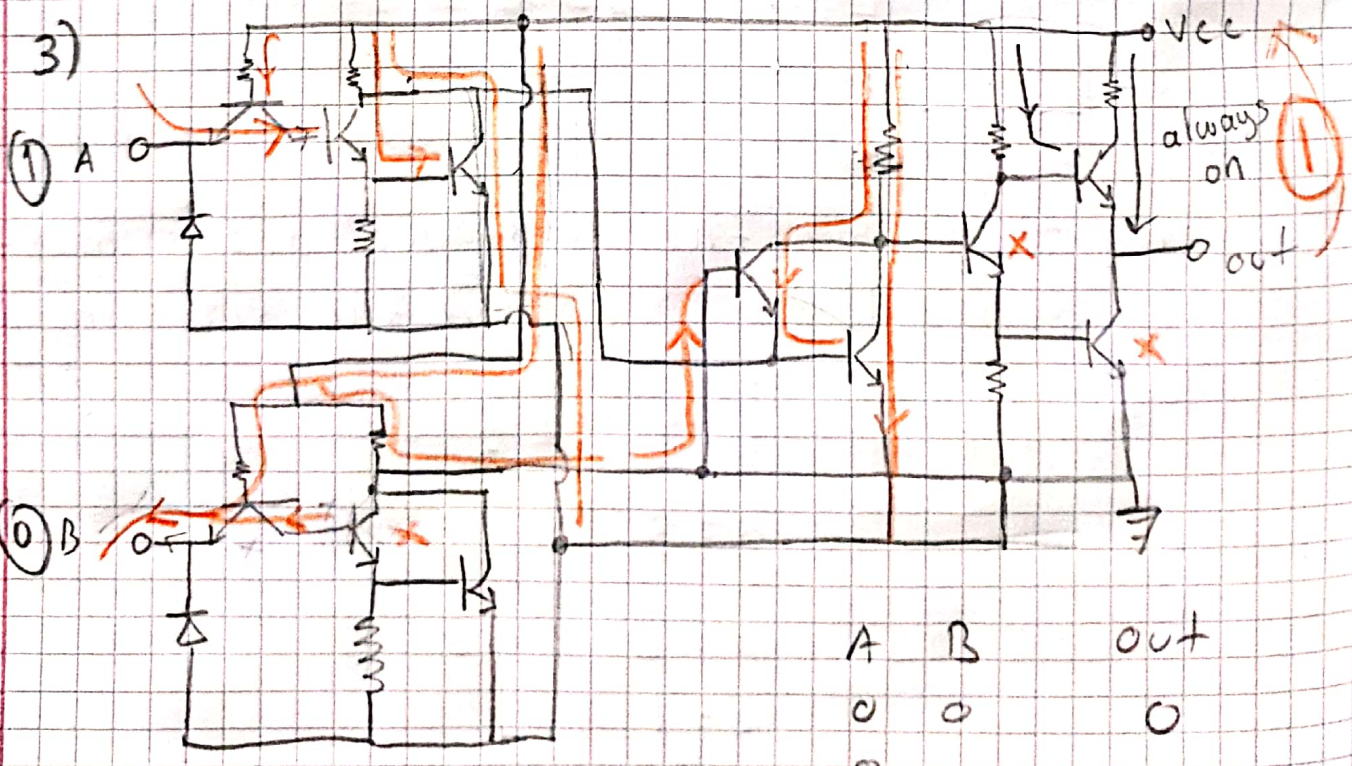
$+ bc'd$ removes hazard

d) $F = a'c' + abc$



No Hazard

3)



A	B	out
0	0	0
0	1	1
1	0	1
1	1	0

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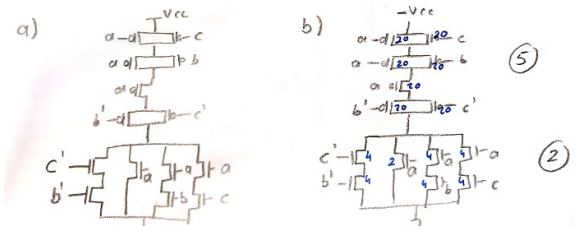
EE 468 COMPUTER ARCHITECTURE FINAL EXAM

PLEASE WRITE YOUR ANSWERS IN THE GIVEN BOXES. THE ANSWERS OUTSIDE THE BOXES WILL NOT BE EVALUATED

1) **(10 p)** a) Design a CMOS circuit that implements F= (c'b'+ a +ab+ac)'

(10 p) b) Adjust the sizes of the circuit in a) for 5/2 pmos/nmos inverter sizing ratio

(15 p) c) Calculate the logical efford (g) for the circuit



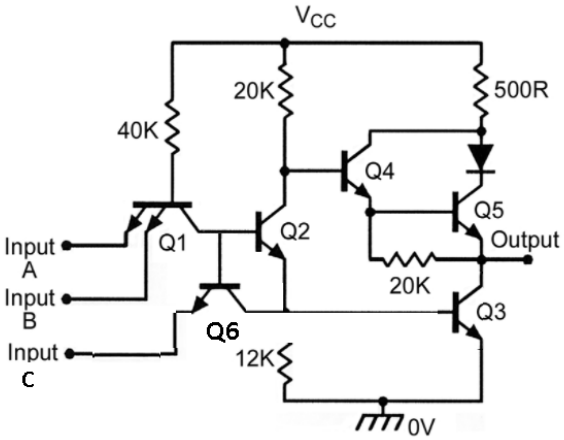
C) (5+2) Cunit g=1

. (20+4) Cunit g=x

- ----------

X=24/7

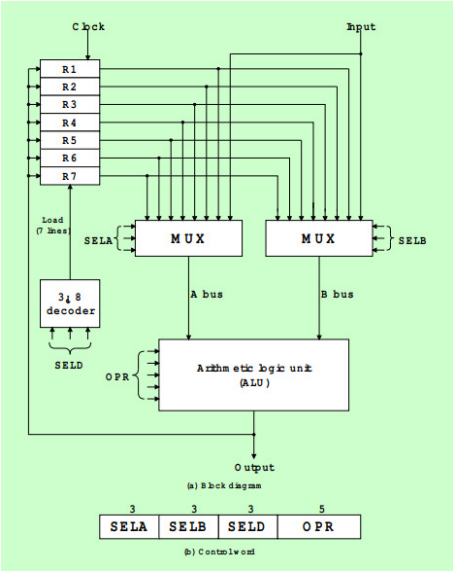
2) **(35 p)** Evaluate the truth table for the given TTL circuit below



A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

3) **(30p)** Write with a sentence, what does the given 14 bits code below do if its a statement of a CPU?

Code: **01010101001010**



- Encoding of the register selection fields

Binary code	SELA	SELB	SELD
000	External input	External input	External input
001	R1	R1	R1
010	R2	R2	R2
011	R3	R3	R3
100	R4	R4	R4
101	R5	R5	R5
110	R6	R6	R6
111	R7	R7	R7

- Encoding of the ALU operation field

OPR select	Operation	Symbol
00000	Transfer A	TSFA
00001	Increment A	INCA
00010	Add A + B	ADD
00101	Subtract A - B	SUB
00110	Decrement A	DECA
01000	AND A and B	AND
01010	OR A and B	OR
01100	XOR A and B	XOR
01110	Complement A	COMA
10000	Shift right A	SHRA
11000	Shift left A	SHLA

Answer : This code is ;

010 101 010 01010

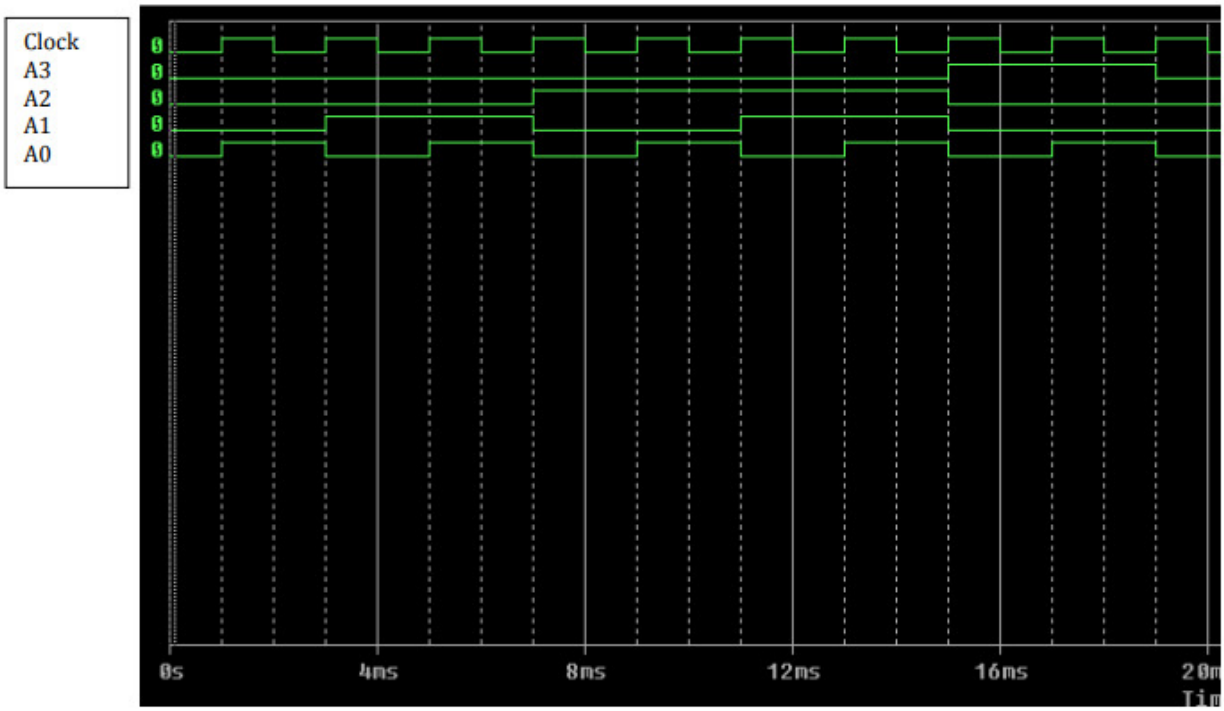
R2 R5 R2 OR which logically ORs the value in R2 and R5 and restores the result in R2

i.e : **R2=R2 OR R5**

Name Surname : **11.01.2022**

ID :

EE 468 COMPUTER ARCHITECTURE LAB EXAM



To evaluate the output given above in ORCAD; after designing the circuit what adjustements should be made in ORCAD (including clocks, flipflops simulation run time etc…) please list them down…

ANSWER

Create new simulation profile
Adjust CLK off time : 1ms
CLK on time : 1ms
Edit simulation profile and adjust simulaiton run time :20 ms
Adjust all FF initial states to 0 in the options part of simulation profile
Place probes to Q points of the FF's